R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus for generating a region of graphics on a display. The apparatus generally comprises a bus, a plurality of registers, a memory, a calculation circuit and a control circuit. The bus may have a first address range and a second address range. The registers may be within the first address range and configured to store an X coordinate and a Y coordinate of a pixel to be drawn on the display. The memory may be directly connected to the bus and responsive within the second address range. The calculation circuit may be configured to calculate an address in the second address range for storage of data corresponding to the pixel in dependence on the X and the Y coordinates. The control circuit may be configured to control writing of the data in the memory across the bus by driving the address onto the bus.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 5 lines 11-14, page 8 lines 5-10, page 17 lines 11-25 and FIGS. 2 and 5 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 3-7, 20-22 and 30 under 35 U.S.C. §103(a) as being unpatentable over Murphy '919 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 8-10 and 23-24 under 35 U.S.C. §103(a) as being unpatentable over Murphy in view of Chiu '391 is respectfully traversed and should be withdrawn.

The rejection of claims 11, 13, 14, 25 and 26 under 35 U.S.C. §103(a) as being unpatentable over Murphy in view of Prouty '658 is respectfully traversed and should be withdrawn.

The rejection of claims 15-19 and 27-29 under 35 U.S.C. §103(a) as being unpatentable over Murphy in view of Ozcelik, Patent Publication No. 2002/0149626 has been obviated by appropriate amendment and should be withdrawn.

Murphy concerns a graphics system with optimized use of unified local and frame buffers (Title). Chiu concerns a scaleable refresh display controller (Title). Prouty concerns a method and apparatus for raster computer graphic display of rotation invariant line styles (Title). Ozcelik concerns a display unit architecture (Title). Murphy, Chiu, Prouty and Ozcelik, alone or in combination, do not appear to teach or suggest every element as claimed. As such, the claimed invention is fully patentable over the cited reference and the rejections should be withdrawn.

Claim 1 provides a memory directly connected to a bus for storing data corresponding to a pixel. In contrast, FIG. 2B of Murphy shows that a local buffer memory is not directly connected to a host bus. The rest of Murphy appears to be silent regarding a memory storing pixel data directly connected to the host bus. Therefore, Murphy does not appear to teach or suggest a memory directly connected to a bus for storing data corresponding to a pixel as presently claimed.

Claim 1 further provides a calculation circuit configured to calculate an address in a second address range of the bus for storage of data. In contrast, Murphy appears to be silent regarding the address calculated by a rasterizer unit (asserted on page 3, lines 6-8 of the Office Action to be similar to the claimed calculation circuit) accounting for any particular address range of the host bus. In particular, column 23, lines 7-8 of Murphy state that the local buffer is accessible within a Region 1 and a Region 3 of a PCI address map for the GLINT graphics processor. However, the address equations in column 27, lines 1-14 of Murphy do not appear to incorporate the base addresses for Region 1 and/or Region 3 of the PCI address map. Therefore, Murphy does not appear to teach or suggest a calculation circuit configured to calculate an address in a second address range of the bus for storage of data as presently claimed.

Claim 1 further provides a control circuit configured to control writing of data in the memory across the bus by driving an address calculated by a calculation circuit onto the bus. In contrast, Murphy appears to be silent regarding a local buffer interface block or any other block controlling writing to memory from across the host bus by driving an address calculated by a rasterizer unit onto the host bus. Therefore, Murphy does not appear to teach or suggest a control circuit configured to control writing of data in the memory across the bus by driving an address calculated by a calculation circuit onto the bus as presently claimed. Claims 15, 20 and 30 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Regarding claim 15, the Office Action has failed to establish *prima facie* obviousness to combine the references. Page 7, paragraph 6 of the Office Action asserts that motivation to combine is to "increase flexibility in defining displays." per paragraph 8 of Ozcelik. The text of Ozcelik cited by the Office Action reads:

> Thus, there is a need for a display hardware that has a relatively low hardware complexity yet provides **substantial** flexibility in defining displays. (Emphasis added)

The above quoted text does not appear to provided any indication that one of ordinary skill in the art would view Ozcelik as a means for **increasing** flexibility in defining displays. The text of

Ozcelik only speaks of providing **substantial** flexibility. No explanation or evidence has been provided in the Office Action why the substantial flexibility of Ozcelik is an increase as compared with what Murphy already teaches. The assertion in the Office Action that Ozcelik would increase a flexibility of Murphy is speculative and lacks supporting evidence. Thus, *prima facie* obviousness to combine the references has not been established for lack of clear and particular evidence for motivation. As such, claim 15 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides a clipping circuit configured to generate a clipping signal. In contrast, Murphy appears to be silent regarding a clipping function of the GLINT graphics processor generating a signal. Furthermore, the Office Action provides no evidence or argument where Murphy indicates generating a clipping signal. Therefore, Murphy does not appear to teach or suggest a clipping circuit configured to generate a clipping signal as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 provides the control circuit is further configured to inhibit writing of data to the address in response to the clipping signal. Page 3, last paragraph of the Office Action admits that Murphy does not teach inhibiting writing. Instead, page 4, lines 2-3 of the Office Action assert that it is inherent

not to process extraneous data. Applicants' representative respectfully traverses the assertion of inherency to not process extraneous data. In particular, column 8, lines 44-48 of Murphy state:

> When the Depth Block receives a message `new fragment`, it will calculate the corresponding depth and do the depth test. If the test passes then the `new fragment` message is passed to the next unit. **If the test fails then the message is modified and passed on.** (Emphasis added)

Since inherency requires certainty of results, not mere possibility, the functionality of Murphy to continue to pass fragments failing the depth test indicates that not processing extraneous data is not a certainty and thus cannot be inherent. Therefore, *prima facie* obviousness to modify Murphy to not write clipped pixel data has not been established. As such, claim 4 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 7 provides a first register memory mapped to a first location and a second location in the first address range of the bus. Despite the assertion on page 4 of the Office Action, the text in column 13, lines 13-18 and 26-28 appear to be silent regarding a register memory mapper to two locations. The text of Murphy cited by the Office Action states:

> When a GLINT host software driver is initialized it can map the register file into its address space. Each register has an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, the tag offset is measured in multiples of 8 bytes).

...
The last write triggers the start of rendering. GLINT has approximately 200 registers.

Nowhere in the above text, or in any other section, does Murphy appear to discuss a register memory mapped to two locations. Therefore, Murphy does not appear to teach or suggest a first register memory mapped to a first location and a second location in a first address range of a bus as presently claimed.

Furthermore, the assertion on page 4 or the Office Action that each register of Murphy has 4 bytes in different locations is moot since the 4 bytes are still within a single register and the single register is at a single address. Nothing in Murphy appears to indicate that any register or sub-portion thereof is mapped to two different addresses on the host bus. Claims 14 and 22 provides language similar to claim 7. As such, claims 7, 14 and 22 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to the control circuit representative of an address location being written to. In contrast, page 4, last paragraph of the Office Action admits that Murphy does not teach an address decoder. Furthermore, the Office Action does not provide any evidence from either reference or knowledge generally available to one of ordinary skill in the art, to modify or combine the

references as required by MPEP §2142. Instead, page 5, lines 7-9 of the Office Action quote language from **Applicants' application** (incorrectly identified as Applicants' amendment) as motivation. However, it is improper to use what the Applicants teach against the Applicants. Therefore, *prima facie* obviousness has not been established to modify Murphy with Chiu for lack of clear and particular evidence compliant with MPEP §2142.

Furthermore, column 3, lines 45-49 and elements 122 and 206 in FIG. 2 of Chiu (cited on page 5, lines 3-4 of the Office Action) appear to be silent regarding monitoring memory locations for a write. Per column 2, line 33 of Chiu, element 122 is a 2-conductor control bus. Element 206 in FIG. 2 of Chiu is an address decoder. The text of Chiu cited in the Office Action reads:

> Address decoder 206 is a binary decoder which produces a load signal on one of four outputs by decoding a two-bit CONTROL signal from decoder 108. The load signals load data from bus 120 into one of the latches 202, 208, 212 and 216.

Nowhere in the above text, or in any other section, does Chiu appear to mention that the address decoder 206 monitors for writes Therefore, Murphy and Chiu, alone or in combination, do not appear to teach or suggest an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to the control circuit representative of an address location being written to as presently claimed. Claim 23 provides language similar to claim 8. As such, claims 8 and 23 are

fully patentable over the cited references and the rejection should be withdrawn.

Clam 14 provides an address decoder. In contrast, page 4, last paragraph of the Office Action admits that Murphy does not teach an address decoder. Likewise, Prouty appears to be silent regarding an address decoder. Furthermore, the assertion on page 6 of the Office Action that claim 14 is rejected for the same reason as claims 8 and 11 is moot as claims 8 and 11 have a different ground of rejection than claim 14. Therefore, Murphy and Prouty, alone or in combination, do not appear to teach or suggest an address decoder as presently claimed.

Furthermore, page 6, first paragraph of the Office Action asserts that motivation to combine Murphy with Prouty would be to "provide for drawing complex line styles in real time." Adding a new capability to an invention because then the invention will have the new capability is circular logic that does not establish motivation. The Office Action has not provided clear and particular evidence why one of ordinary skill in the art would be motivated to modify the teaching of Murphy to add a complex line style drawing capability as taught by Prouty. As such, claim 14 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 16 provides a second register and a logic unit for writing data to the second register. In contrast, both Murphy and

Ozcelik appear to be silent regarding a logic unit writing data to a register. Therefore, Murphy and Ozcelik, alone or in combination, do not appear to teach or suggest a second register and a logic unit for writing data to the second register as presently claimed. As such, claim 16 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 19 provides that the control circuit is further configured to combine data for pixels in response to a receipt of the same address signal. In contrast, both Murphy and Ozcelik appear to be silent regarding a control circuit combining pixel data upon receipt of an address signal. Furthermore, page 8 of the Office Action merely cites the arguments for claim 18 in regards to claim 19. However, the arguments for claim 18 are silent regarding modifications to the local buffer interface block (asserted in the Office Action to be similar to the claimed control circuit) due the addition of a conventional comparator. Therefore, Murphy and Ozcelik, alone or in combination, do not appear to teach or suggest a control circuit configured to combine data for pixels in response to a receipt of a same address signal as presently claimed. Claim 28 provides language similar to claim 19. As such, claims 19 and 28 are fully patentable over the cited reference and the rejection should be withdrawn.

IMPROPERLY EXPRESSED REJECTIONS

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a non-final action due to a lack of proper development for the resent rejections. In particular, Applicants' representative traversed the assertion in the January 29, 2003 previous Office Action that there is clear and particular motivation to combine the primary reference with either Prouty or Ozcelik. MPEP §707.07(f) reads:

> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and **answer the substance** of it. (Emphasis added)

Regarding Prouty, the current Office Action merely repeats the same argument word-for-word from the previous Office Action without addressing the traverse. Regarding Ozcelik, the current Office Action repeats a portion of the argument from the previous Office Action word-for-word without addressing the traverse. As such, the current Office Action is incomplete.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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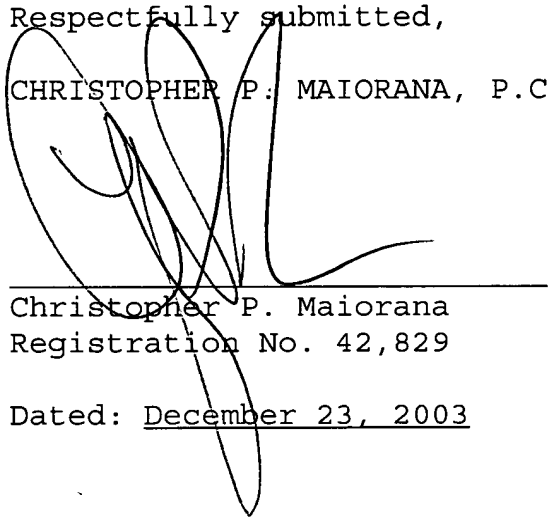

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